IN THE SPECIFICATION

Please replace the paragraphs on page 14, lines 10 through page 15, line 13 as shown below.

Further, processor 401 includes a watchpoint controller 403 that provides control information to a pipeline control unit 409 in order to stall and start an execution pipeline of processor 401. The watchpoint controller 403 may also keep track of watchpoint channel information in processor 401, and provide such information to circuit 402. Processor 401 also includes a branch unit 404 that handles branch-related instructions in processor 401, resolves/predicts branch addresses, and other branch-related functions. Branch unit 404 provides signals program counter information 414, CPU mode information ~~415~~ 421, and branch information ~~416~~ 422. Branch unit 404 also provides process identifier or ASID information 416. Processor 401 also includes a load-store unit 405 which is responsible for performing execution functions. Load-store unit 405 includes operand address (OA) watchpoints 406, which produce operand address information 415.

ASID information 416 and operand address (OA) information 415 are fed through multiplexer 417 and transmitted to debug circuit 402 via data line ~~417~~ 423. In one aspect of the invention, it is understood that when new ASID information 416 is available, no operand address information 415 will be available concurrently. Thus, the number of communication lines in communication link 420 are reduced because both ASID information 416 and OA information 415 are transmitted alternately over the same communication lines.